FIG. 1

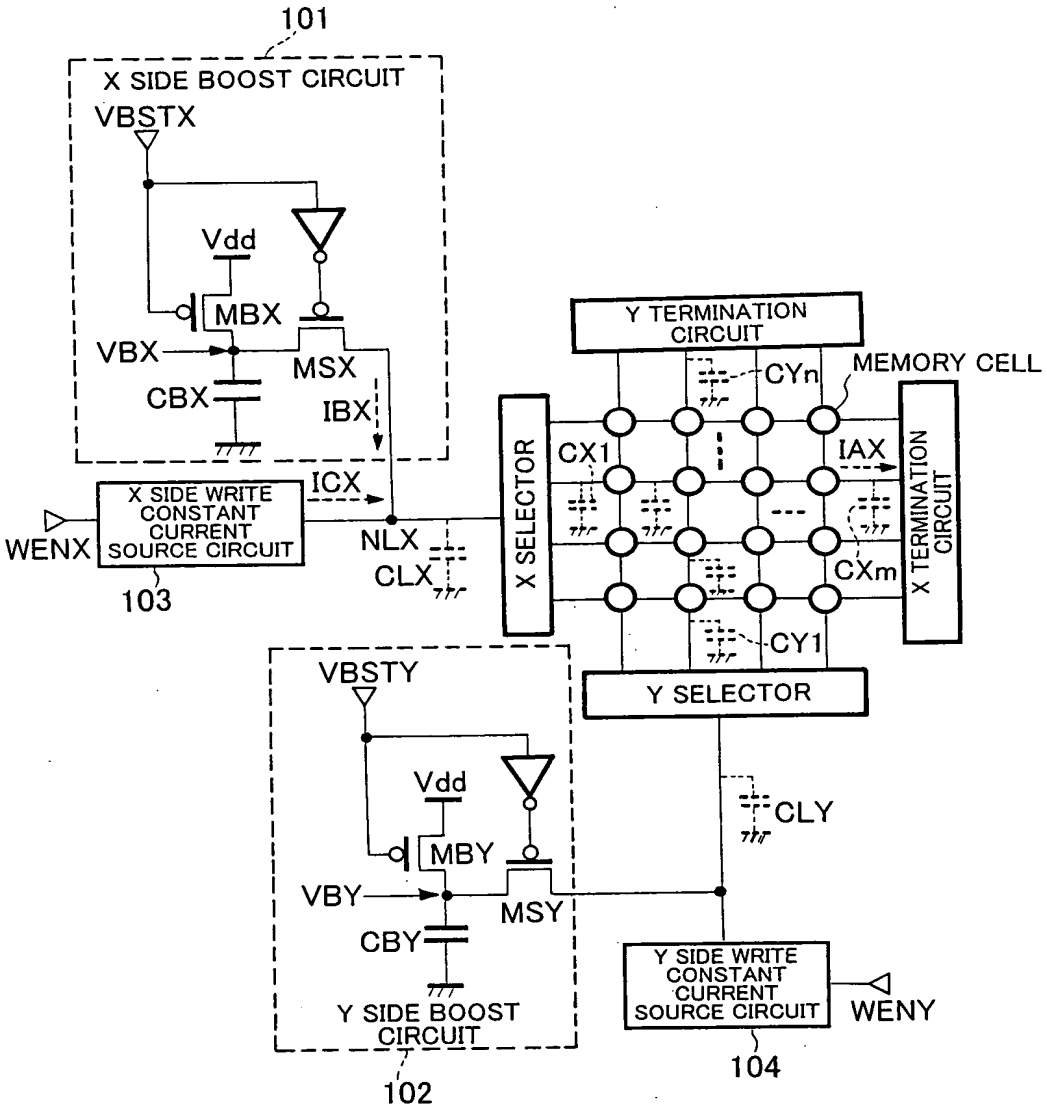

101
X SIDE BOOST CIRCUIT
VBSTX
Vdd
MBX
VBX
MSX
CBX
IBX
ICX
X SIDE WRITE CONSTANT CURRENT SOURCE CIRCUIT
WENX
103
NLX
CLX
X SELECTOR
Y TERMINATION CIRCUIT
CYn
MEMORY CELL
CX1
IAX
CXm
X TERMINATION CIRCUIT
CY1
Y SELECTOR
CLY
VBSTY
Vdd
MBY
VBY
MSY
CBY
Y SIDE BOOST CIRCUIT
102
Y SIDE WRITE CONSTANT CURRENT SOURCE CIRCUIT
WENY
104

FIG.2

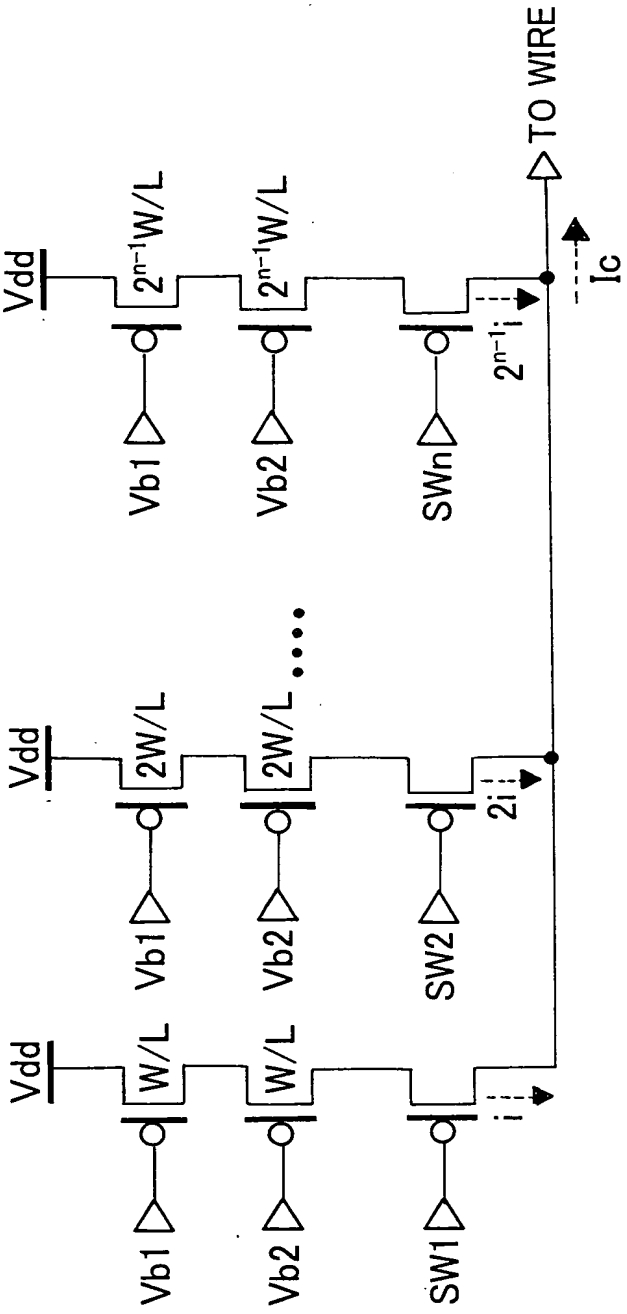


FIG.3A

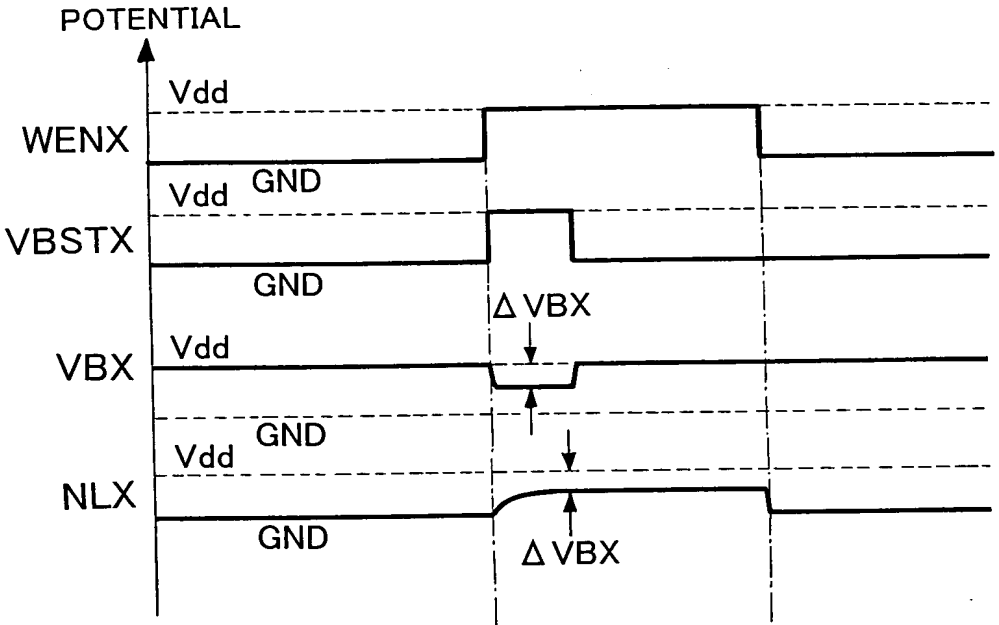

POTENTIAL
Vdd
WENX
Vdd
GND
VBSTX
GND
ΔVBX
VBX
Vdd
GND
Vdd
NLX
GND
ΔVBX

FIG.3B

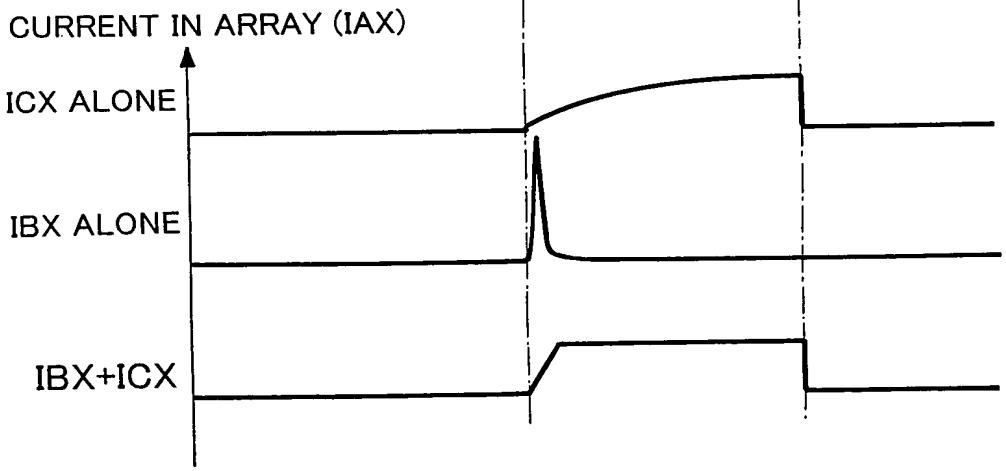

CURRENT IN ARRAY (IAX)
ICX ALONE
IBX ALONE
IBX+ICX

FIG. 4A

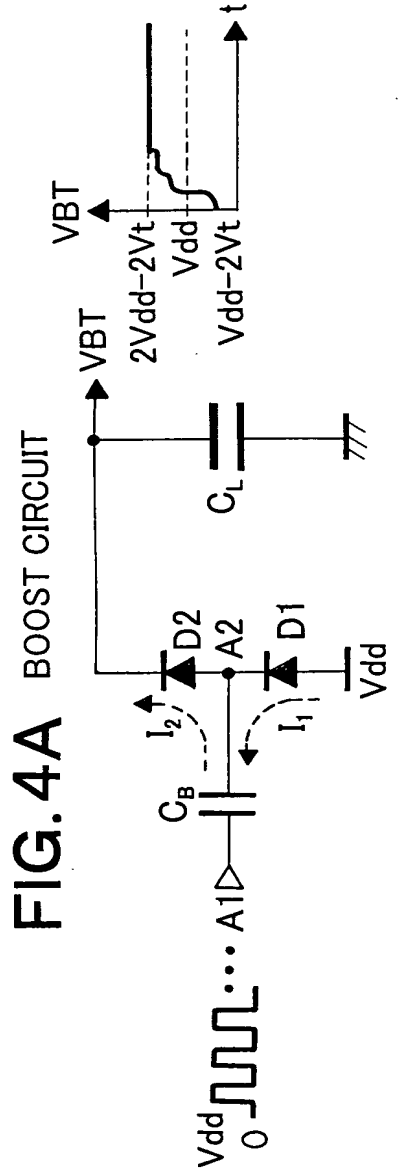

BOOST CIRCUIT
VBT
2Vdd-2Vt
Vdd
Vdd-2Vt
t
VBT
C_L
D2
A2
D1
I_2
I_1
C_B
Vdd
A1
Vdd
0

FIG. 4B

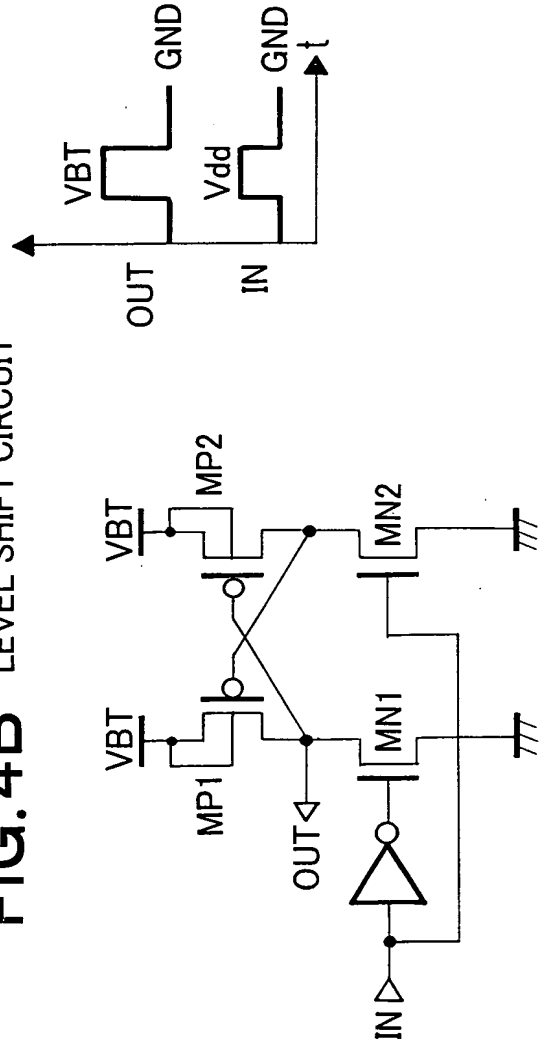

LEVEL SHIFT CIRCUIT
VBT
GND
Vdd
GND
t
OUT
IN
VBT
MP2
MN2
VBT
MP1
MN1
OUT
IN

FIG.5

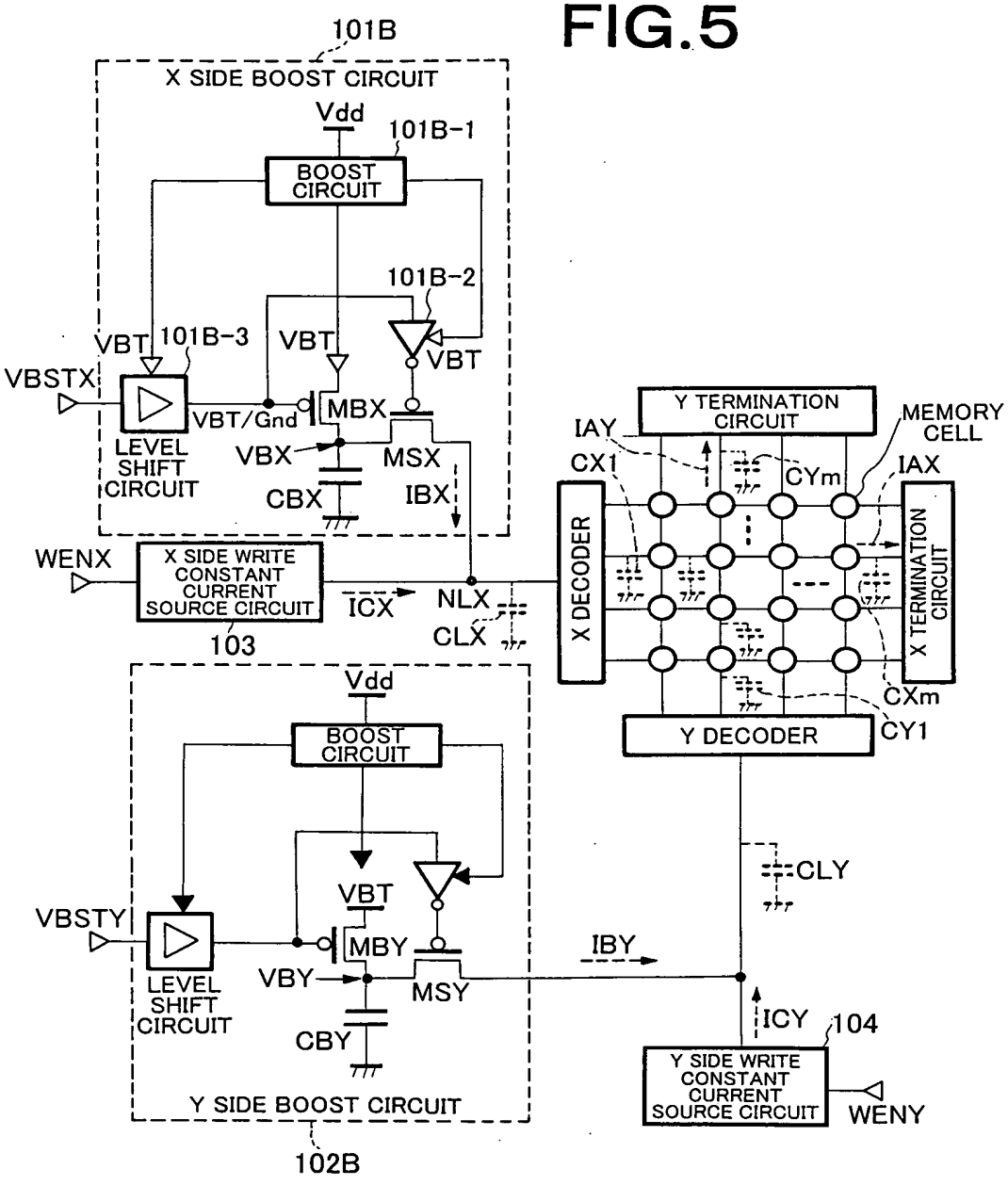

101B
X SIDE BOOST CIRCUIT
Vdd
101B-1
BOOST CIRCUIT
101B-2
VBT
101B-3
VBT
VBT
VBSTX
LEVEL SHIFT CIRCUIT
VBT/Gnd
MBX
VBX
MSX
CBX
IBX
WENX
X SIDE WRITE CONSTANT CURRENT SOURCE CIRCUIT
103
ICX
NLX
CLX
Y TERMINATION CIRCUIT
MEMORY CELL
IAY
CX1
CYm
IAX
X DECODER
X TERMINATION CIRCUIT
CXm
Y DECODER
CY1
Vdd
BOOST CIRCUIT
VBT
VBSTY
LEVEL SHIFT CIRCUIT
MBY
VBY
MSY
CBY
IBY
CLY
ICY
104
Y SIDE WRITE CONSTANT CURRENT SOURCE CIRCUIT
WENY
Y SIDE BOOST CIRCUIT
102B

FIG.6A

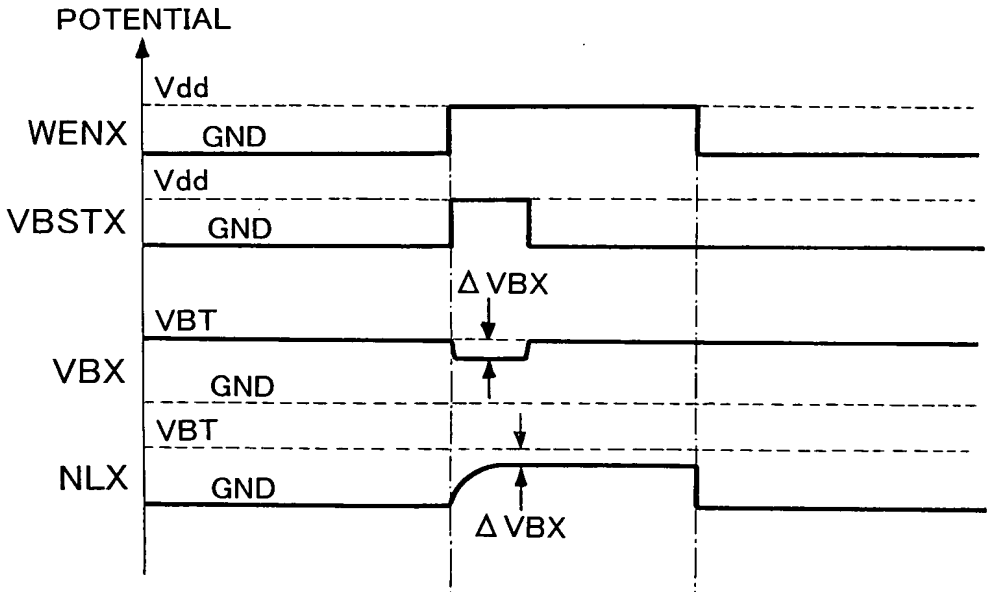

POTENTIAL
Vdd
WENX
GND
Vdd
VBSTX
GND
ΔVBX
VBT
VBX
GND
VBT
NLX
GND
ΔVBX

FIG.6B

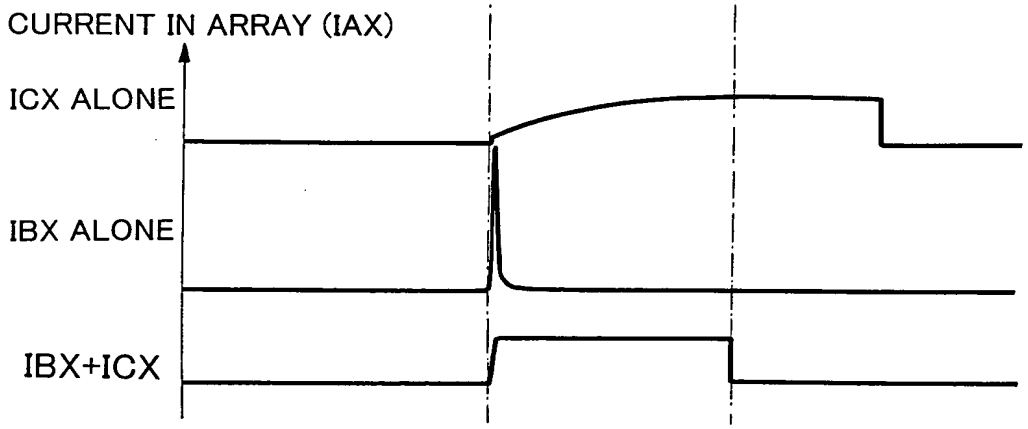

CURRENT IN ARRAY (IAX)
ICX ALONE
IBX ALONE
IBX+ICX

FIG. 7

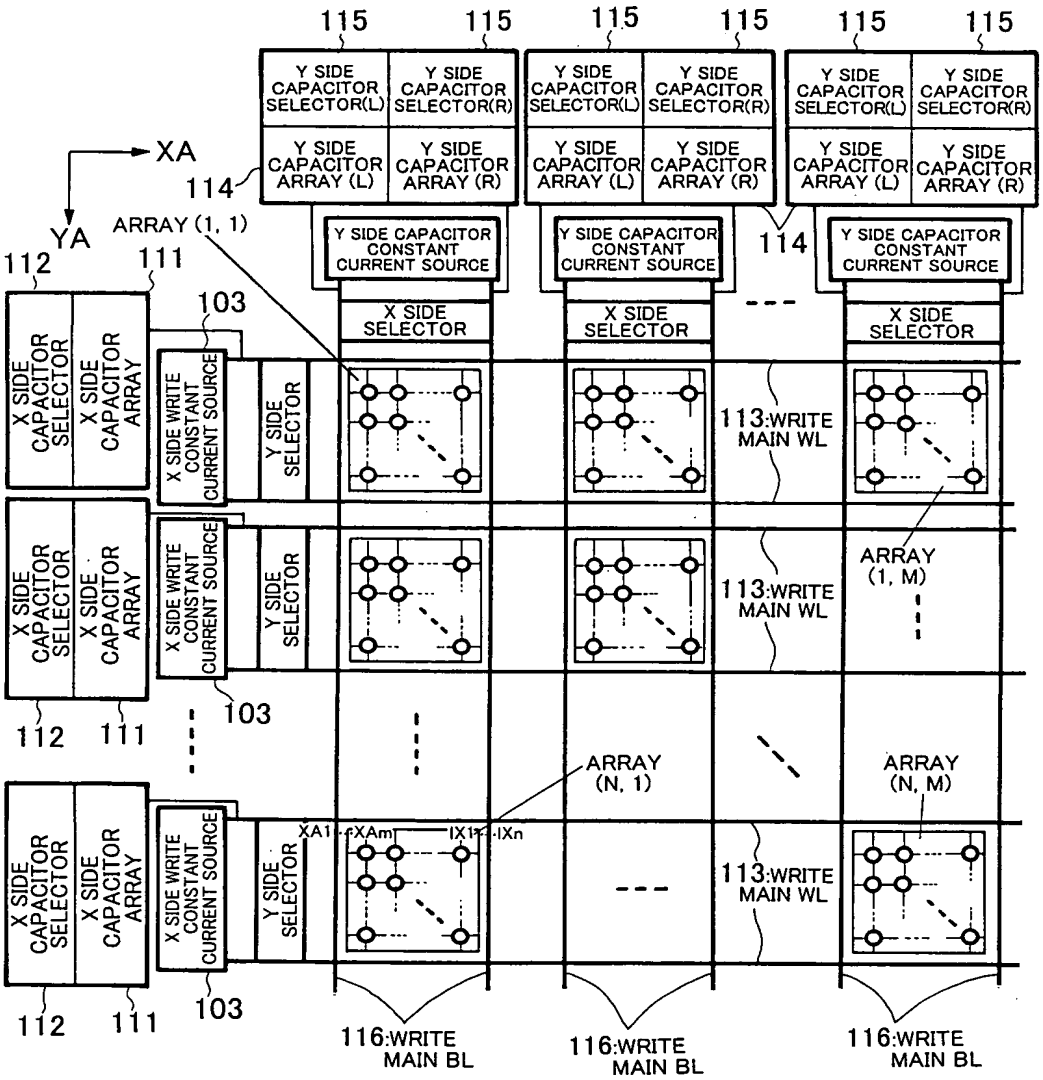

115
Y SIDE CAPACITOR SELECTOR(L)
Y SIDE CAPACITOR SELECTOR(R)
Y SIDE CAPACITOR ARRAY (L)
Y SIDE CAPACITOR ARRAY (R)
114
XA
YA
ARRAY (1, 1)
112
111
103
Y SIDE CAPACITOR CONSTANT CURRENT SOURCE
X SIDE SELECTOR
X SIDE CAPACITOR SELECTOR
X SIDE CAPACITOR ARRAY
X SIDE WRITE CONSTANT CURRENT SOURCE
Y SIDE SELECTOR
113:WRITE MAIN WL
ARRAY (1, M)
ARRAY (N, 1)
ARRAY (N, M)
XA1
XAm
IX1
IXn
116:WRITE MAIN BL

FIG.8

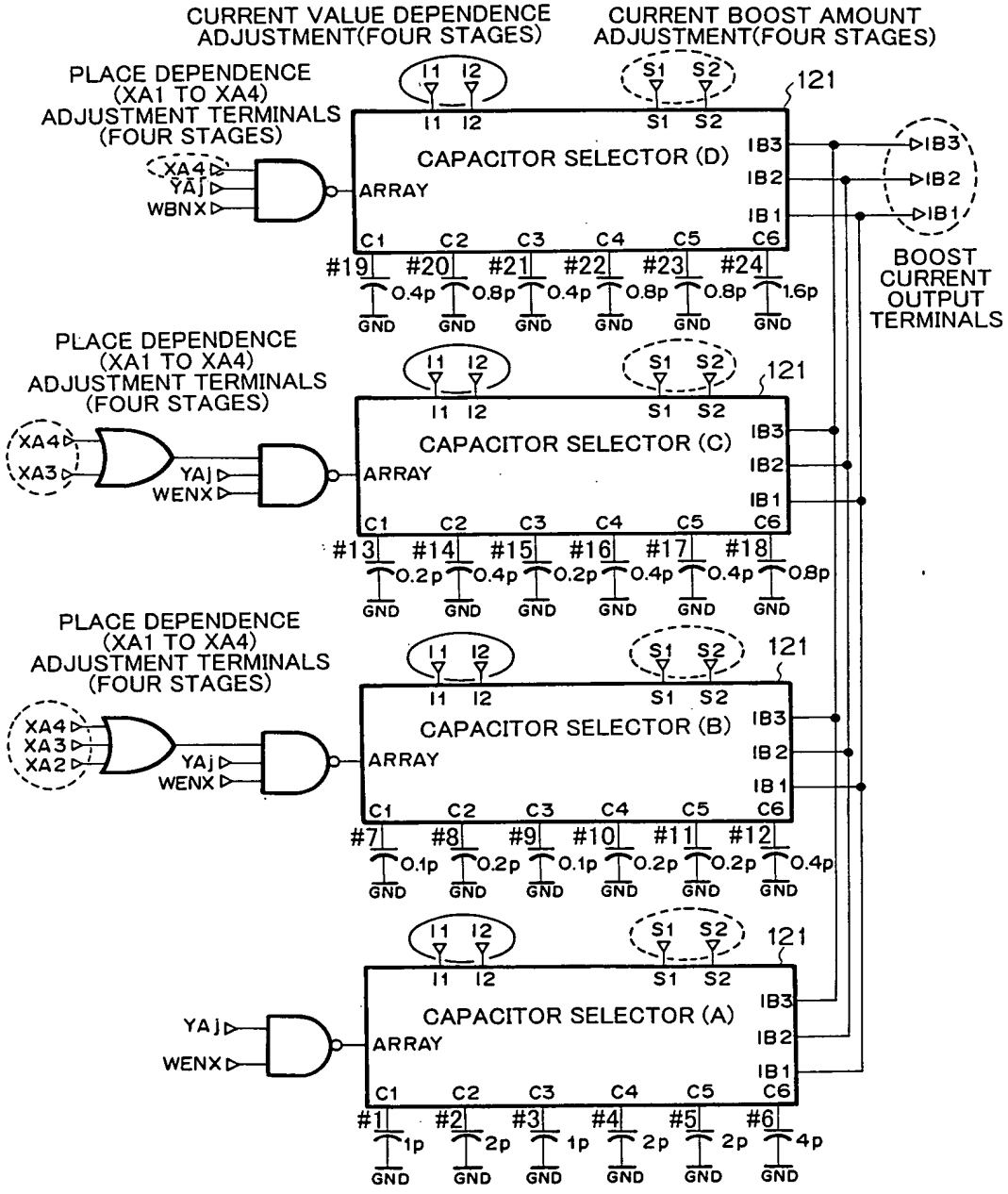

CURRENT VALUE DEPENDENCE ADJUSTMENT(FOUR STAGES)
CURRENT BOOST AMOUNT ADJUSTMENT(FOUR STAGES)
PLACE DEPENDENCE (XA1 TO XA4) ADJUSTMENT TERMINALS (FOUR STAGES)
I1 I2
S1 S2
121
CAPACITOR SELECTOR (D)
CAPACITOR SELECTOR (C)
CAPACITOR SELECTOR (B)
CAPACITOR SELECTOR (A)
ARRAY
XA4
XA3
XA2
YAj
WBNX
WENX
IB3
IB2
IB1
C1 C2 C3 C4 C5 C6
#19 #20 #21 #22 #23 #24
0.4p 0.8p 0.4p 0.8p 0.8p 1.6p
#13 #14 #15 #16 #17 #18
0.2p 0.4p 0.2p 0.4p 0.4p 0.8p
#7 #8 #9 #10 #11 #12
0.1p 0.2p 0.1p 0.2p 0.2p 0.4p
#1 #2 #3 #4 #5 #6
1p 2p 1p 2p 2p 4p
GND
BOOST CURRENT OUTPUT TERMINALS

FIG.9

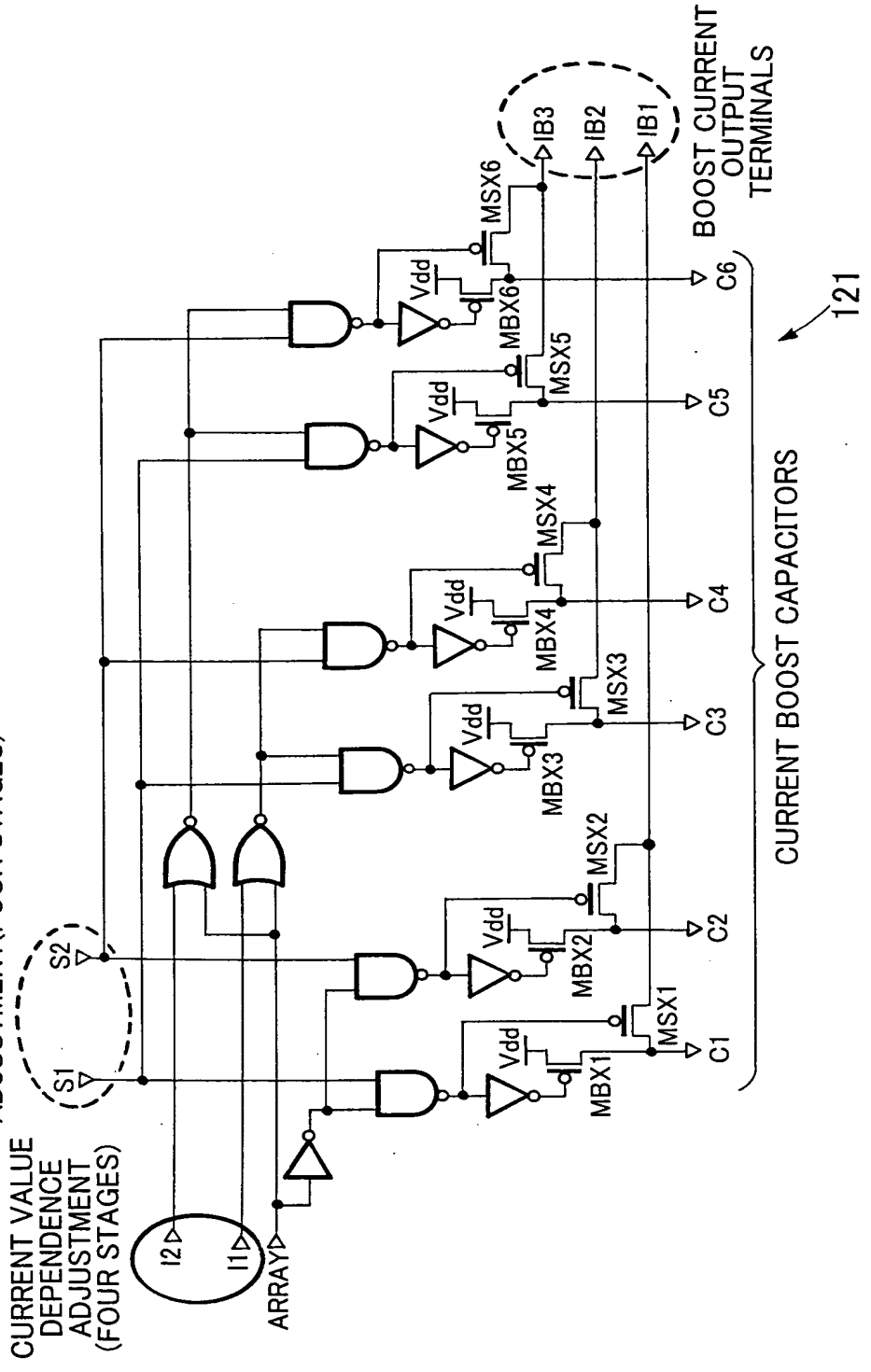

CURRENT BOOST AMOUNT ADJUSTMENT(FOUR STAGES)
S2
S1
CURRENT VALUE DEPENDENCE ADJUSTMENT (FOUR STAGES)
I2
I1
ARRAY
Vdd
MBX1
MBX2
MBX3
MBX4
MBX5
MBX6
MSX1
MSX2
MSX3
MSX4
MSX5
MSX6
C1
C2
C3
C4
C5
C6
IB1
IB2
IB3
BOOST CURRENT OUTPUT TERMINALS
CURRENT BOOST CAPACITORS
121

FIG.10

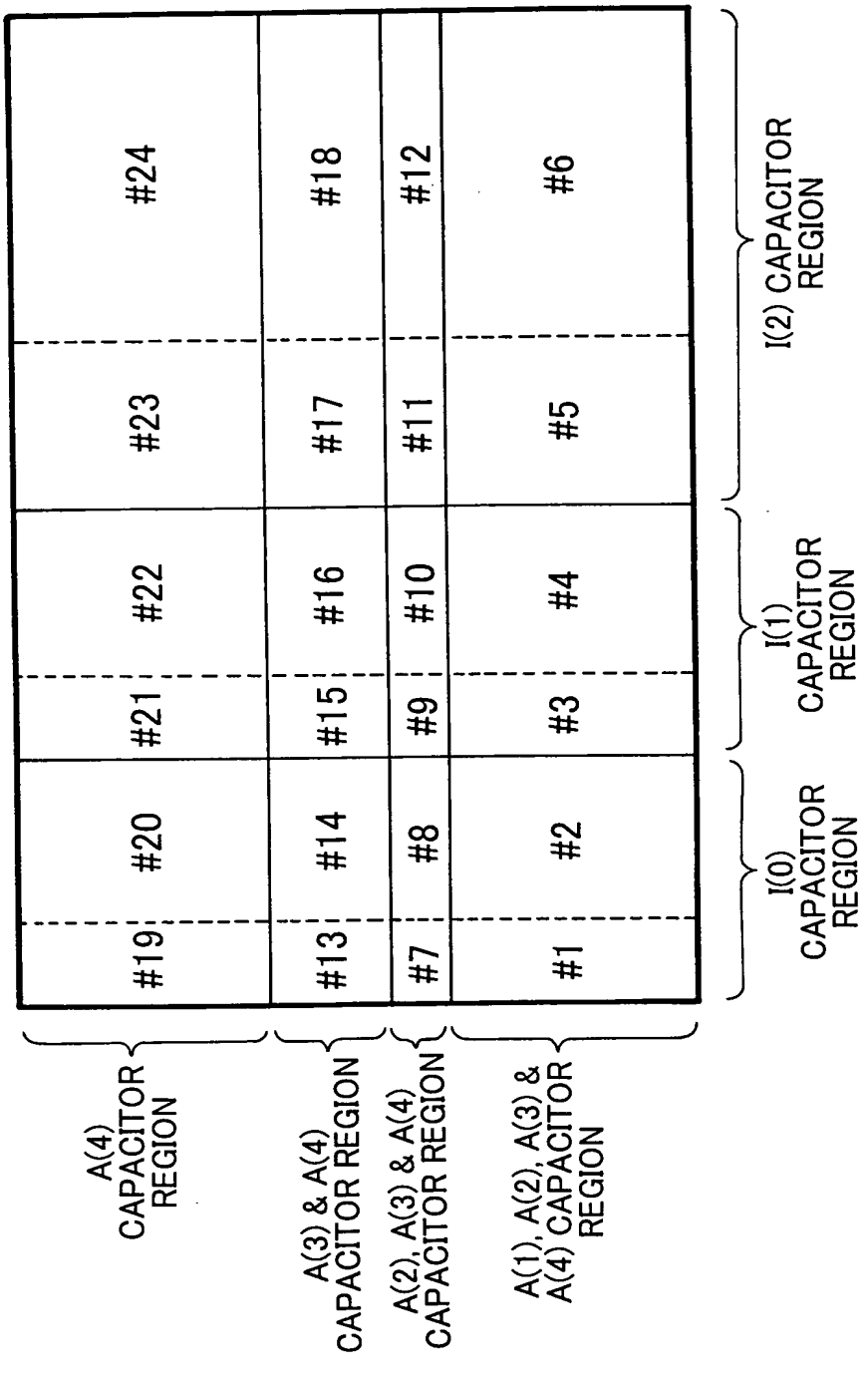

I(3) CAPACITOR REGION
#19
#20
#21
#22
#23
#24
#13
#14
#15
#16
#17
#18
#7
#8
#9
#10
#11
#12
#1
#2
#3
#4
#5
#6
A(4) CAPACITOR REGION
A(3) & A(4) CAPACITOR REGION
A(2), A(3) & A(4) CAPACITOR REGION
A(1), A(2), A(3) & A(4) CAPACITOR REGION
I(0) CAPACITOR REGION
I(1) CAPACITOR REGION
I(2) CAPACITOR REGION

FIG.11

	CURRENT (3:0)	ARRAY (4:1)	ADJUST-MENT (3:0)	CAPACI-TANCE (PF)	CAPACITORS TO BE USED
1	I(0)	A(1)	S(0)	0.0	NOTHING
2	I(0)	A(1)	S(1)	1.0	#1
3	I(0)	A(1)	S(2)	2.0	#2
4	I(0)	A(1)	S(3)	3.0	#1,#2
5	I(0)	A(2)	S(0)	0.0	NOTHING
6	I(0)	A(2)	S(1)	1.1	#1,#7
7	I(0)	A(2)	S(2)	2.2	#2,#8
8	I(0)	A(2)	S(3)	3.3	#1,#2,#7,#8
9	I(0)	A(3)	S(0)	0.0	NOTHING
10	I(0)	A(3)	S(1)	1.3	#1,#7,#13
11	I(0)	A(3)	S(2)	2.6	#2,#8,#14
12	I(0)	A(3)	S(3)	3.9	#1,#2,#7,#8,#13,#14
13	I(0)	A(4)	S(0)	0.0	NOTHING
14	I(0)	A(4)	S(1)	1.5	#1,#7,#13,#19
15	I(0)	A(4)	S(2)	3.0	#2,#8,#14,#20
16	I(0)	A(4)	S(3)	4.5	#1,#2,#7,#8,#13,#14,#19,#20
17	I(1)	A(1)	S(0)	0.0	NOTHING
18	I(1)	A(1)	S(1)	2.0	#1,#3
19	I(1)	A(1)	S(2)	4.0	#2,#4
20	I(1)	A(1)	S(3)	6.0	#1-#4
21	I(1)	A(2)	S(0)	0.0	NOTHING
22	I(1)	A(2)	S(1)	2.2	#1,#3,#7,#9
23	I(1)	A(2)	S(2)	4.4	#2,#4,#8,#10
24	I(1)	A(2)	S(3)	6.6	#1,#2,#7,#8
25	I(1)	A(3)	S(0)	0.0	NOTHING
26	I(1)	A(3)	S(1)	2.6	#1,#3,#7,#9,#13,#15
27	I(1)	A(3)	S(2)	5.2	#2,#4,#8,#10,#14,#16
28	I(1)	A(3)	S(3)	7.8	#1-#4,#7-#10,#13-#16
29	I(1)	A(4)	S(0)	0.0	NOTHING
30	I(1)	A(4)	S(1)	3.4	#1,#3,#7,#9,#13,#15,#19,#21
31	I(1)	A(4)	S(2)	7.8	#2,#4,#8,#10,#14,#16,#20,#22
32	I(1)	A(4)	S(3)	11.2	#1-#4,#7-#10,#13-#16,#19-#22
33	I(2)	A(1)	S(0)	0.0	NOTHING
34	I(2)	A(1)	S(1)	3.0	#1,#5
35	I(2)	A(1)	S(2)	6.0	#2,#6
36	I(2)	A(1)	S(3)	9.0	#1,#2,#5,#6
37	I(2)	A(2)	S(0)	0.0	NOTHING
38	I(2)	A(2)	S(1)	3.3	#1,#5,#7,#11
39	I(2)	A(2)	S(2)	6.6	#2,#6,#8,#12
40	I(2)	A(2)	S(3)	9.9	#1,#2,#5,#6,#7,#8,#11,#12
41	I(2)	A(3)	S(0)	0.0	NOTHING
42	I(2)	A(3)	S(1)	3.9	#1,#5,#7,#11,#13,#17
43	I(2)	A(3)	S(2)	7.8	#2,#6,#8,#12,#14,#18
44	I(2)	A(3)	S(3)	11.7	#1,#2,#5-#8,#11-#14,#17,#18
45	I(2)	A(4)	S(0)	0.0	NOTHING
46	I(2)	A(4)	S(1)	5.1	#1,#5,#7,#11,#13,#17,#19,#23
47	I(2)	A(4)	S(2)	10.2	#2,#6,#8,#12,#14,#18,#20,#24
48	I(2)	A(4)	S(3)	15.3	#1,#2,#5-#8,#11-#14,#17-#20,#23,#24
49	I(3)	A(1)	S(0)	0.0	NOTHING
50	I(3)	A(1)	S(1)	4.0	#1,#3,#5
51	I(3)	A(1)	S(2)	8.0	#2,#4,#6
52	I(3)	A(1)	S(3)	120	#1-#6
53	I(3)	A(2)	S(0)	0.0	NOTHING
54	I(3)	A(2)	S(1)	4.4	#1,#3,#5,#7,#9,#11
55	I(3)	A(2)	S(2)	8.8	#2,#4,#6,#8,#10,#12
56	I(3)	A(2)	S(3)	13.2	#1-#12
57	I(3)	A(3)	S(0)	0.0	NOTHING
58	I(3)	A(3)	S(1)	5.2	#1,#3,#5,#7,#9,#11,#13,#15,#17
59	I(3)	A(3)	S(2)	10.4	#2,#4,#6,#8,#10,#12,#14,#16,#18
60	I(3)	A(3)	S(3)	15.6	#1-#18
61	I(3)	A(4)	S(0)	0.0	NOTHING
62	I(3)	A(4)	S(1)	6.8	#1,#3,#5,#7,#9,#11,#13,#15,#17,#19,#21,#23
63	I(3)	A(4)	S(2)	13.6	#2,#4,#6,#8,#10,#12,#14,#16,#18,#20,#22,#24
64	I(3)	A(4)	S(3)	20.4	#1-#24

FIG.12A

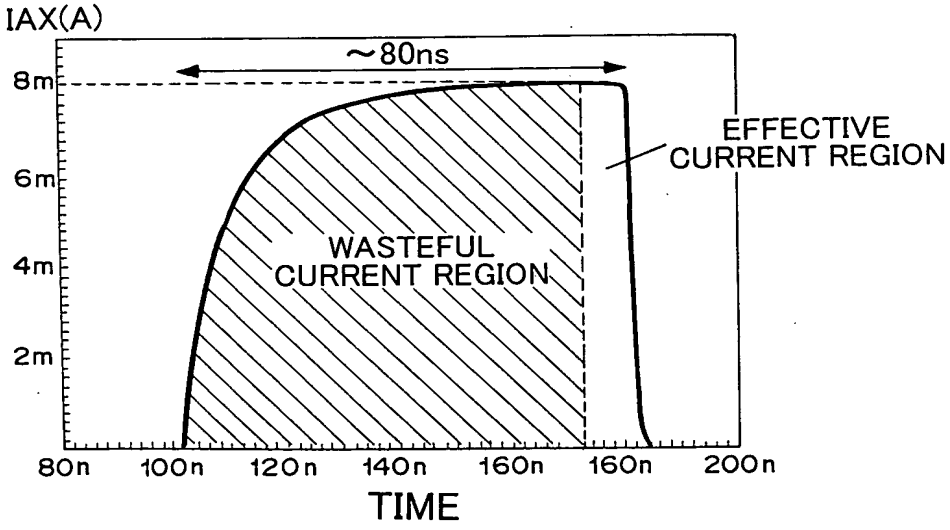


FIG.12B

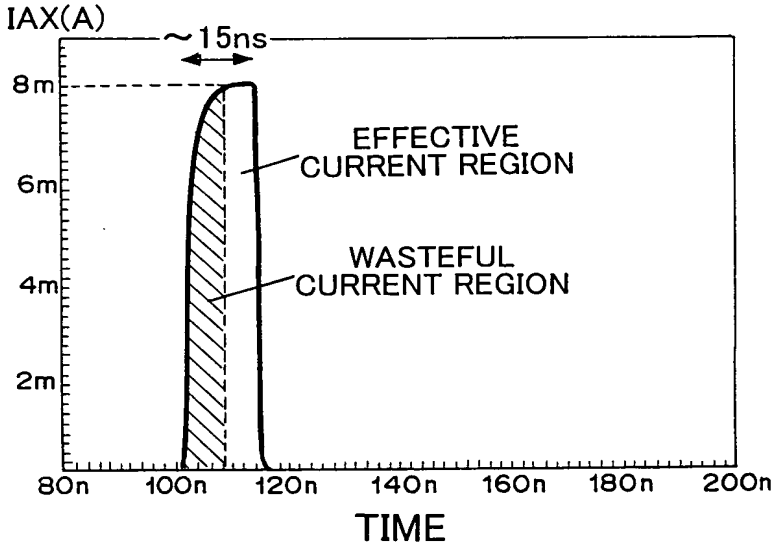


FIG.13

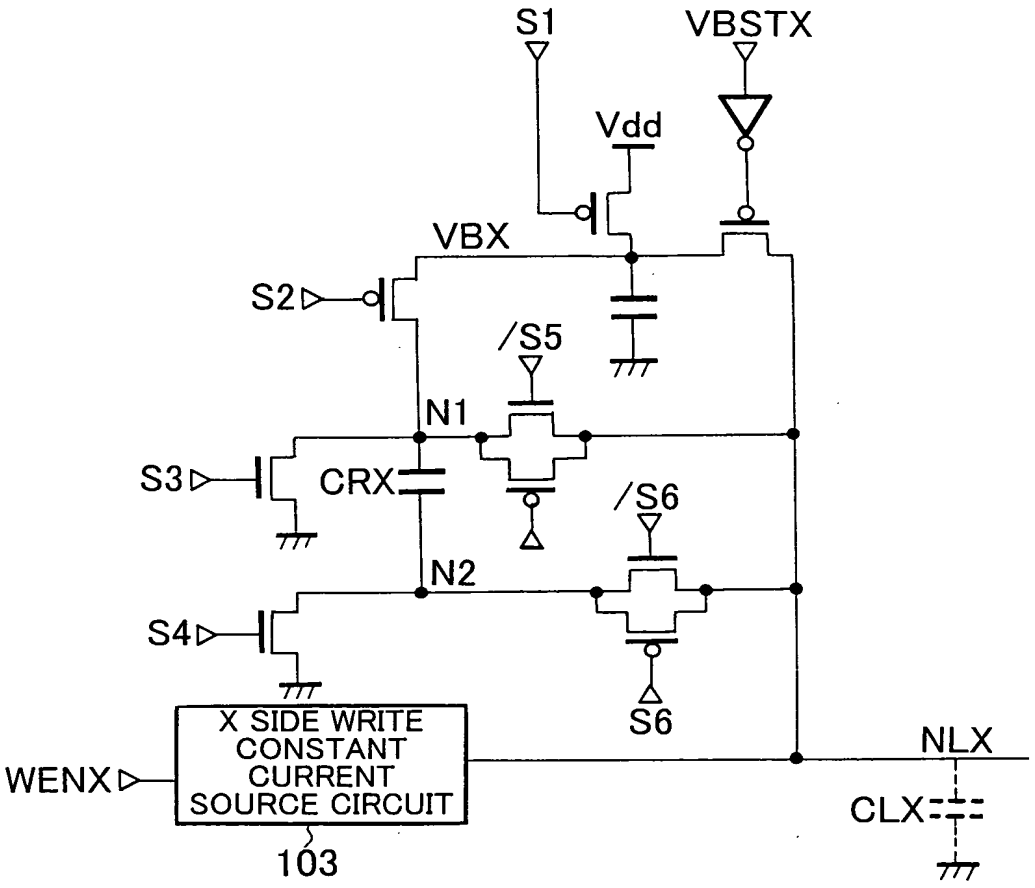

S1
VBSTX
Vdd
VBX
S2
/S5
N1
S3
CRX
/S6
N2
S4
S6
X SIDE WRITE CONSTANT CURRENT SOURCE CIRCUIT
WENX
NLX
CLX
103

FIG.14

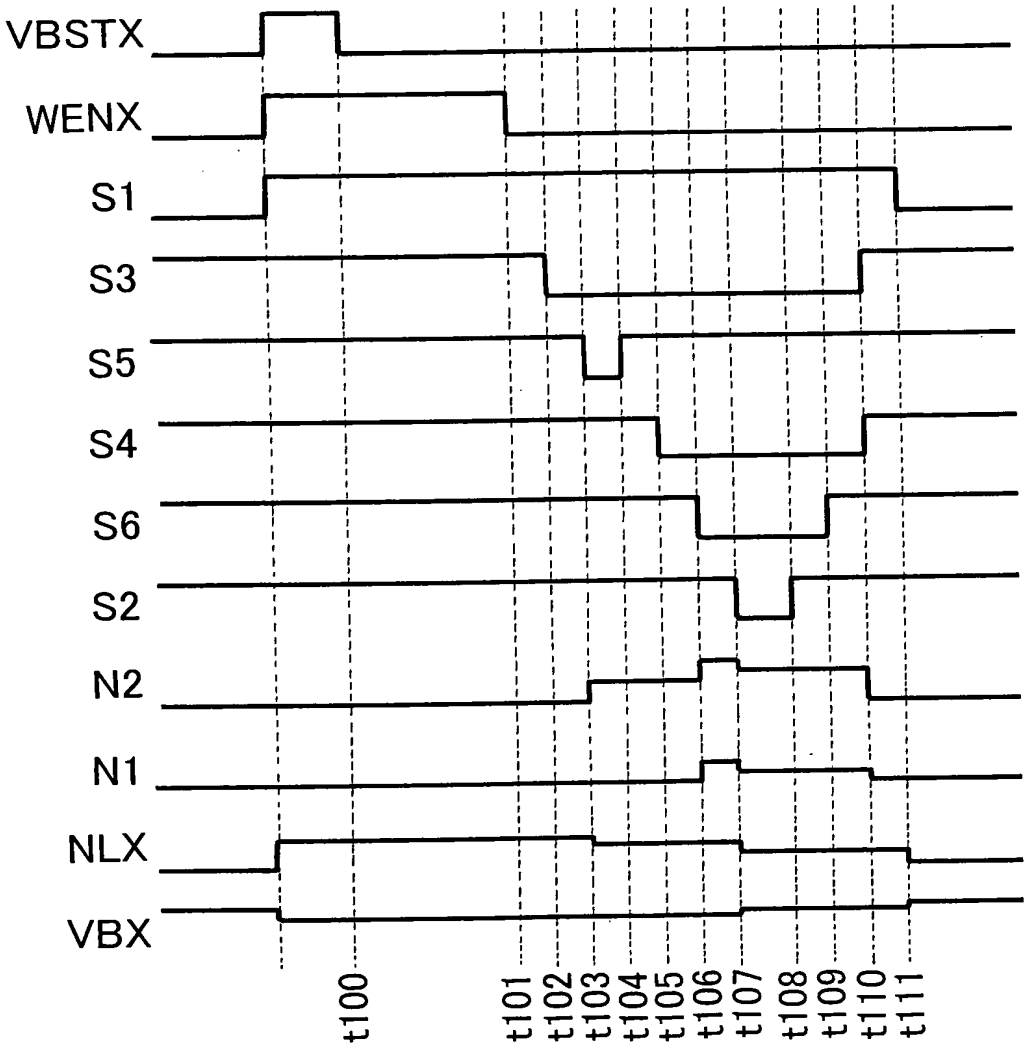

VBSTX
WENX
S1
S3
S5
S4
S6
S2
N2
N1
NLX
VBX
t100
t101
t102
t103
t104
t105
t106
t107
t108
t109
t110
t111

FIG.15

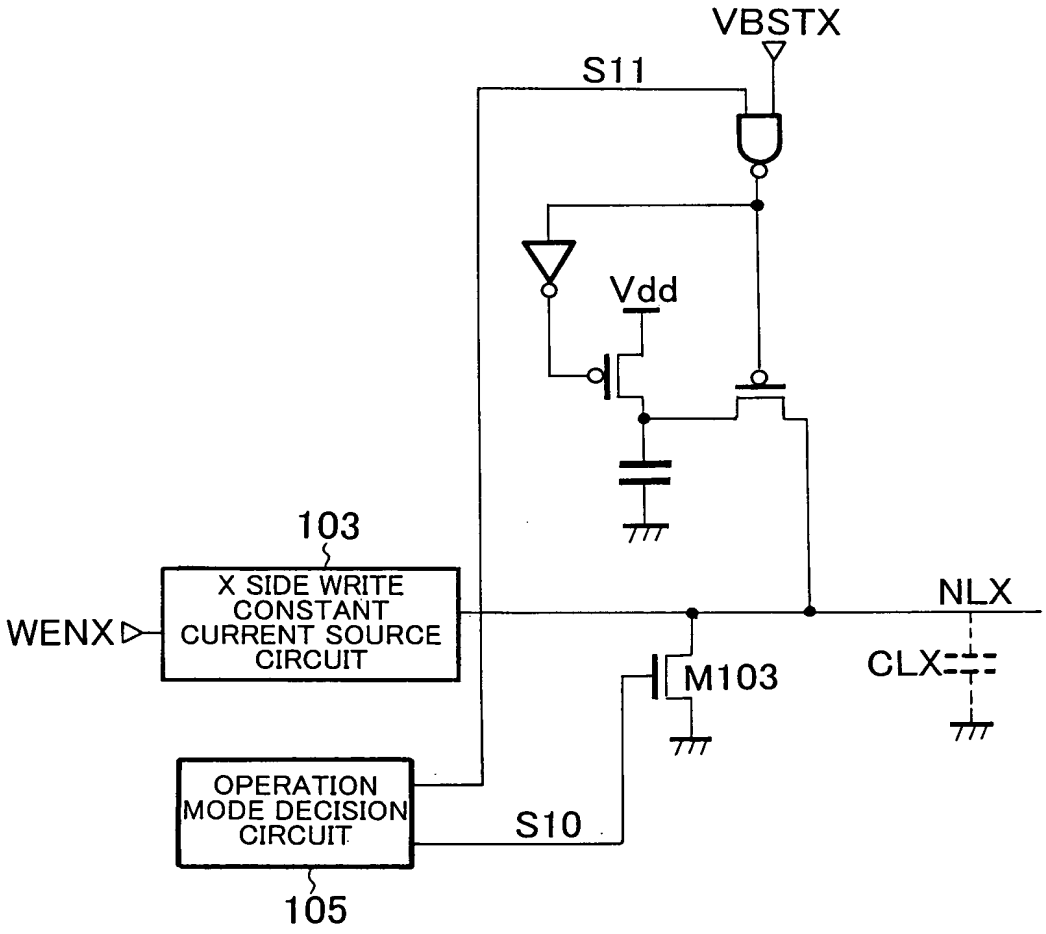

VBSTX
S11
Vdd
103
X SIDE WRITE CONSTANT CURRENT SOURCE CIRCUIT
WENX
NLX
M103
CLX
OPERATION MODE DECISION CIRCUIT
S10
105

FIG.16

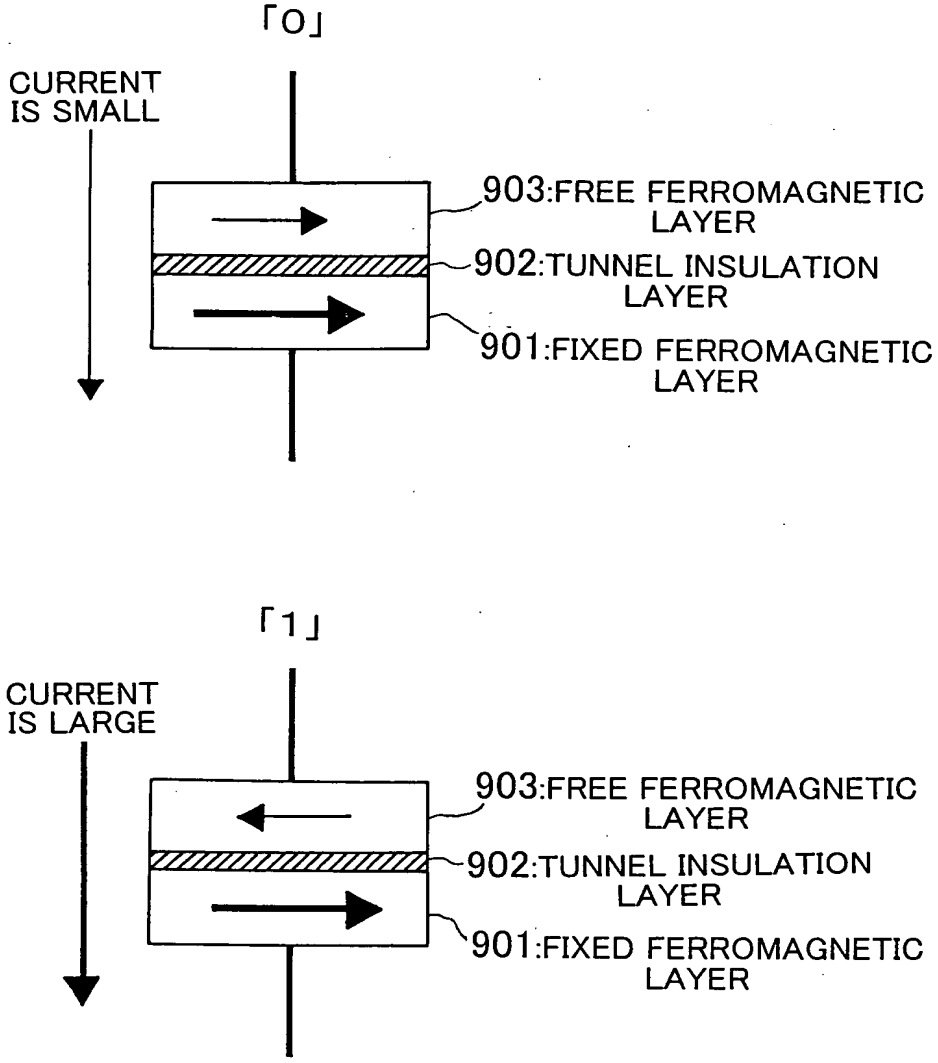

「0」
CURRENT IS SMALL
903:FREE FERROMAGNETIC LAYER
902:TUNNEL INSULATION LAYER
901:FIXED FERROMAGNETIC LAYER
「1」
CURRENT IS LARGE
903:FREE FERROMAGNETIC LAYER
902:TUNNEL INSULATION LAYER
901:FIXED FERROMAGNETIC LAYER

FIG.17A

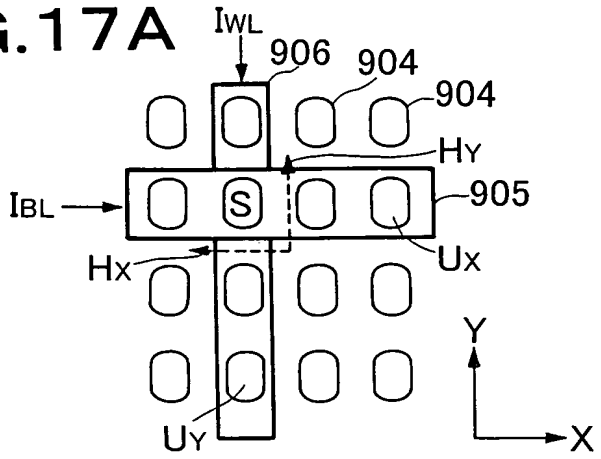


FIG.17B

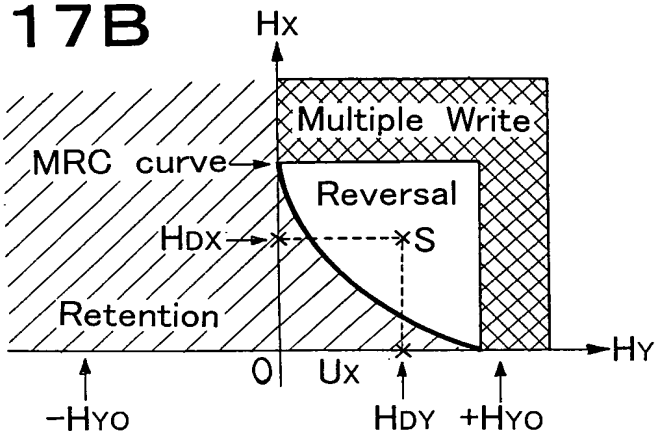


FIG.17C

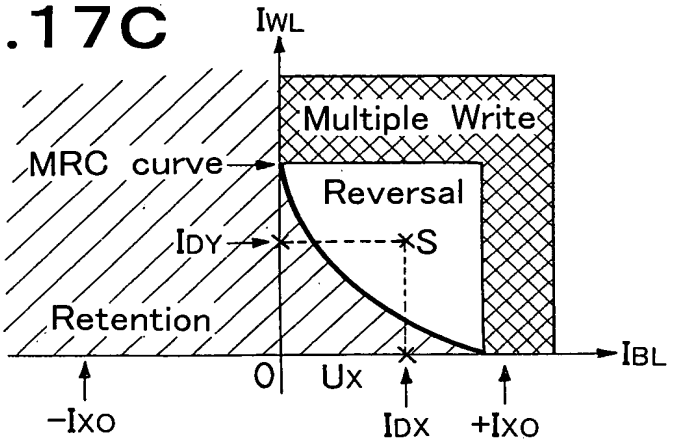
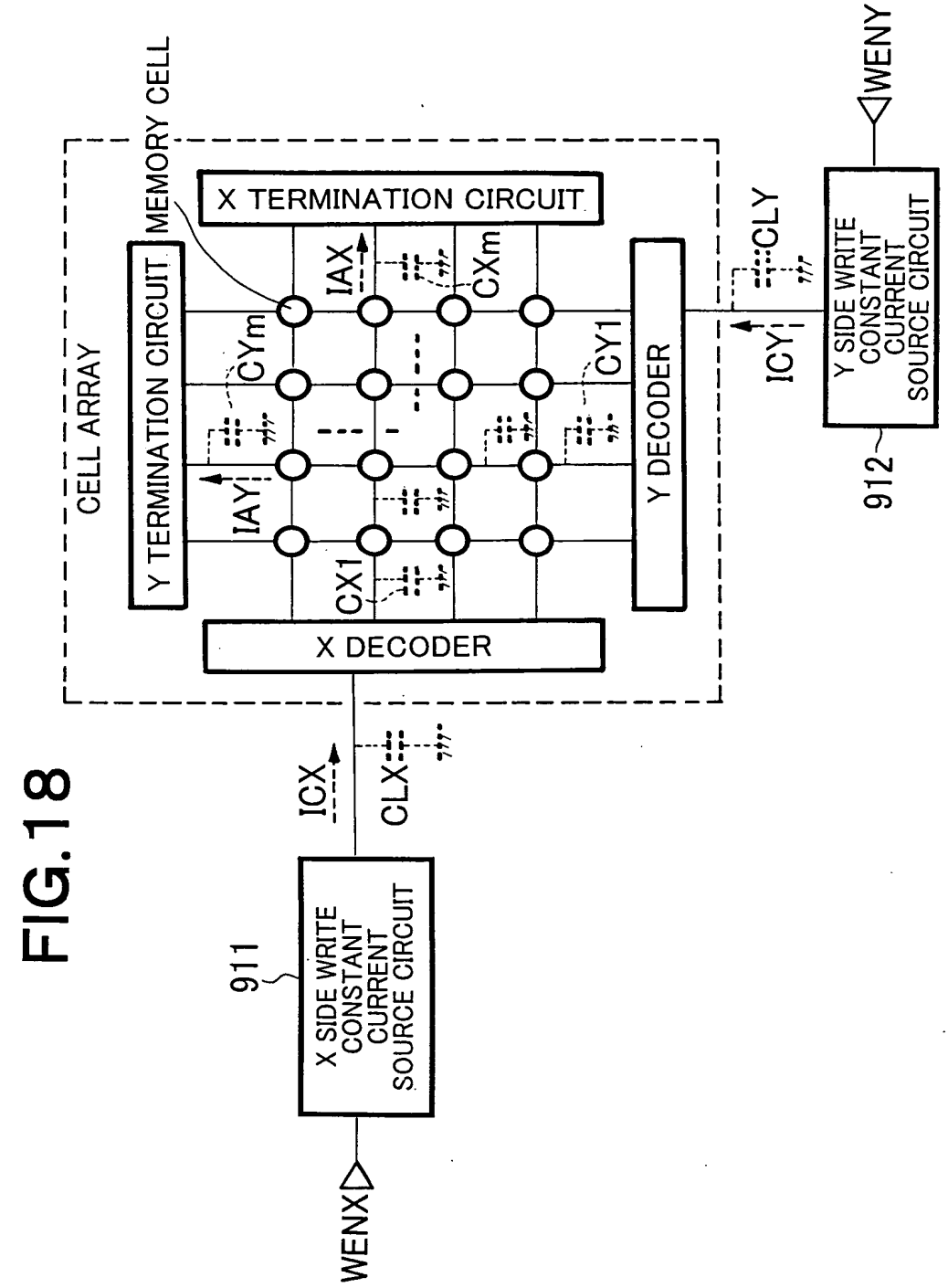


FIG.18


MEMORY CELL
CELL ARRAY
X TERMINATION CIRCUIT
Y TERMINATION CIRCUIT
Y DECODER
X DECODER
IAX
IAY
CXm
CX1
CYm
CY1
ICX
CLX
ICY
CLY
WENX
WENY
911
912
X SIDE WRITE CONSTANT CURRENT SOURCE CIRCUIT
Y SIDE WRITE CONSTANT CURRENT SOURCE CIRCUIT

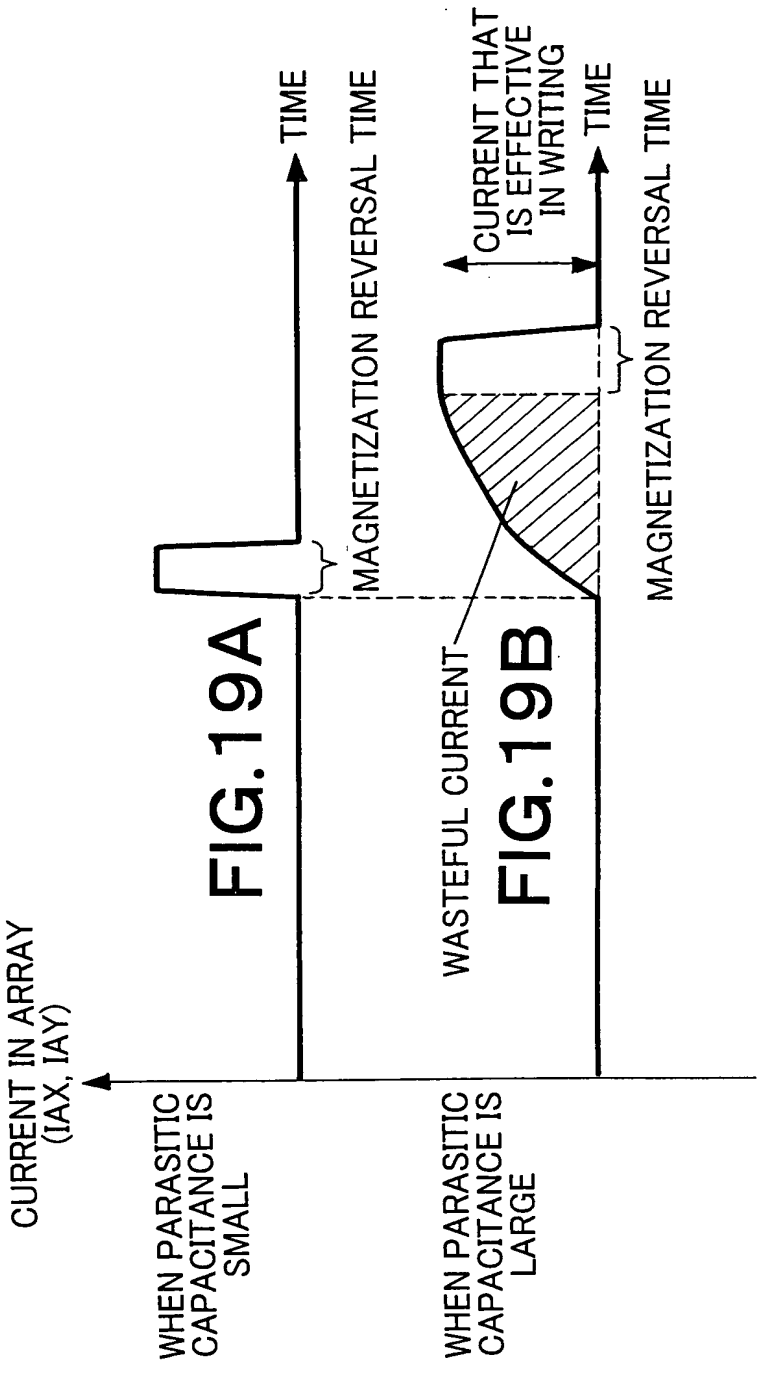


FIG.19A

FIG.19B

FIG.20

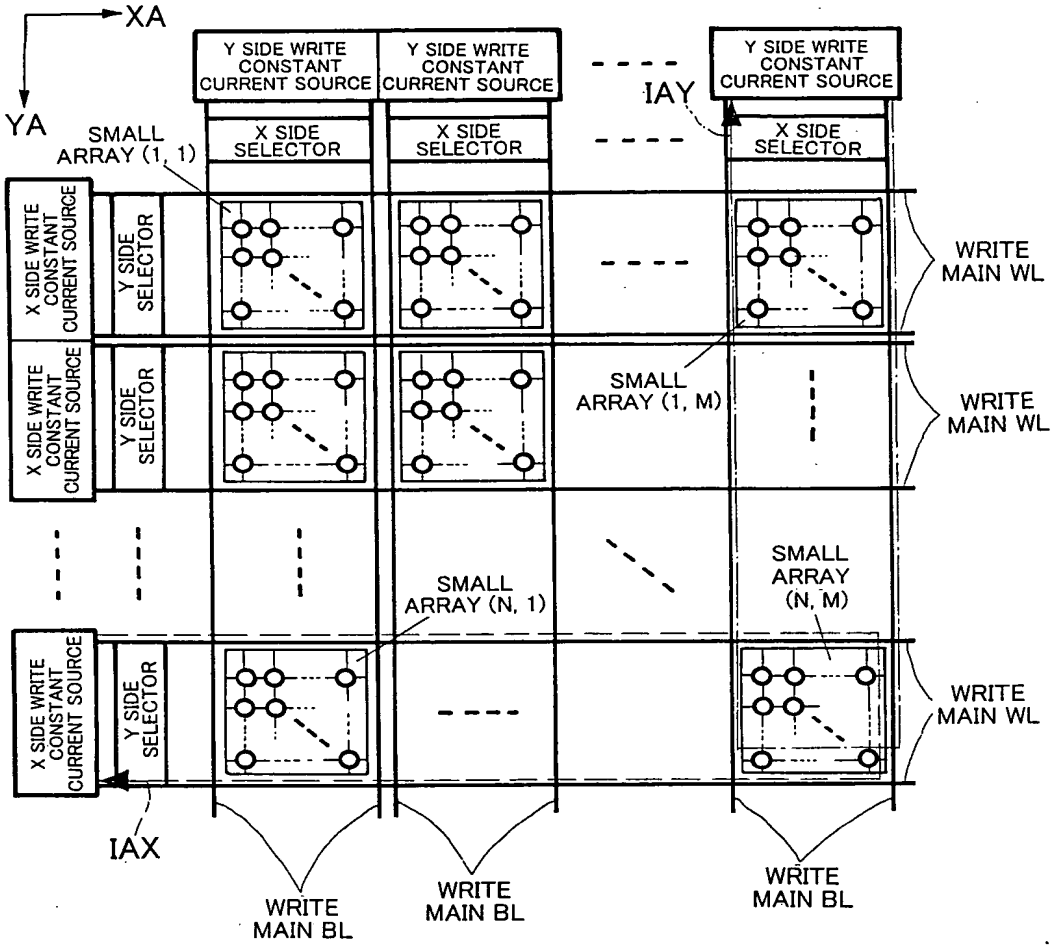
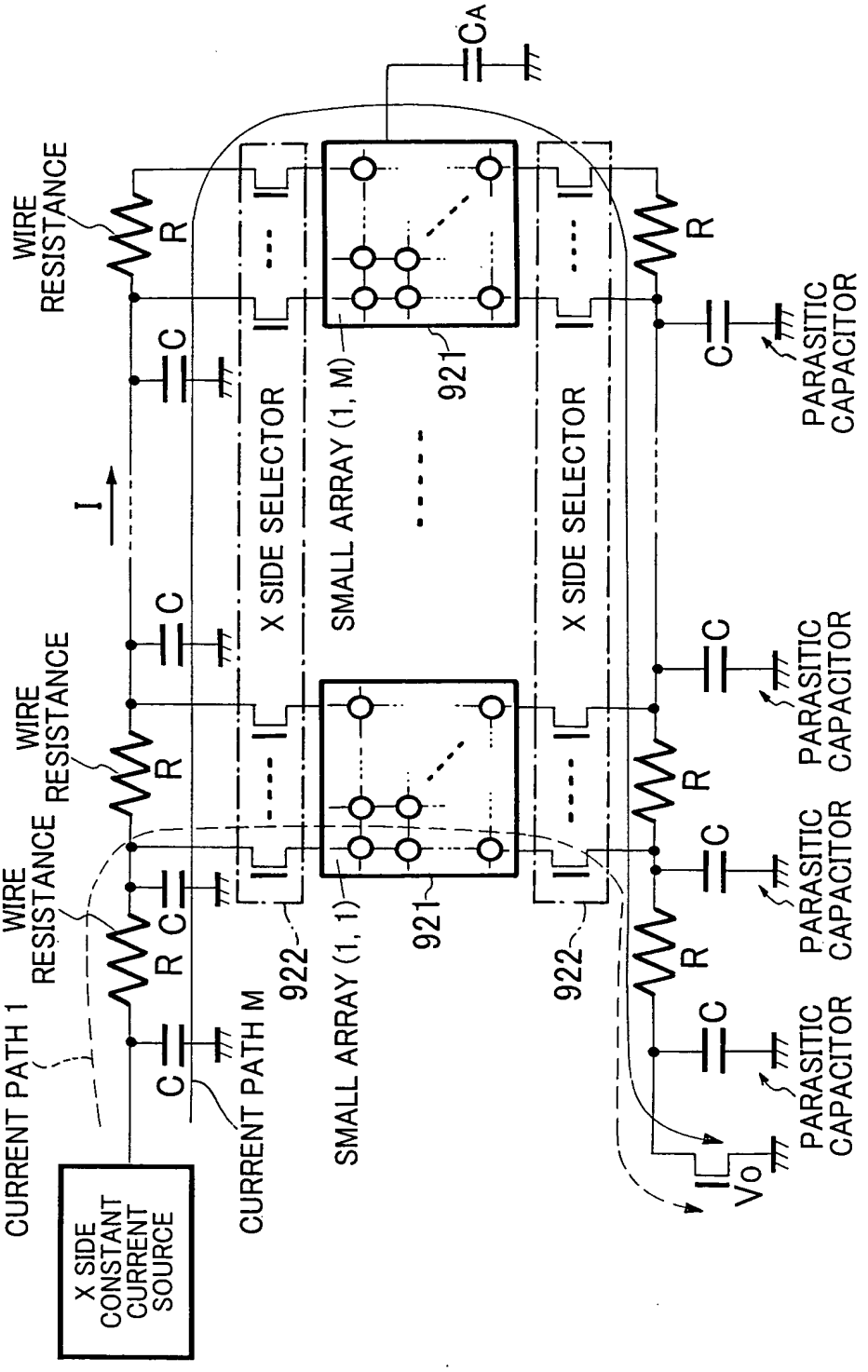

XA
YA
Y SIDE WRITE CONSTANT CURRENT SOURCE
Y SIDE WRITE CONSTANT CURRENT SOURCE
Y SIDE WRITE CONSTANT CURRENT SOURCE
IAY
X SIDE SELECTOR
X SIDE SELECTOR
X SIDE SELECTOR
SMALL ARRAY (1, 1)
X SIDE WRITE CONSTANT CURRENT SOURCE
Y SIDE SELECTOR
WRITE MAIN WL
X SIDE WRITE CONSTANT CURRENT SOURCE
Y SIDE SELECTOR
SMALL ARRAY (1, M)
WRITE MAIN WL
SMALL ARRAY (N, 1)
SMALL ARRAY (N, M)
X SIDE WRITE CONSTANT CURRENT SOURCE
Y SIDE SELECTOR
WRITE MAIN WL
IAX
WRITE MAIN BL
WRITE MAIN BL
WRITE MAIN BL

FIG.21


CA
WIRE RESISTANCE
R
C
X SIDE SELECTOR
SMALL ARRAY (1, M)
921
PARASITIC CAPACITOR
I
CURRENT PATH 1
CURRENT PATH M
X SIDE CONSTANT CURRENT SOURCE
SMALL ARRAY (1, 1)
922
Vo